

## REMARKS

Receipt of the Office Action of March 25, 2005 is gratefully acknowledge.

Claims 1 and 2 have been examined. These have been rejected as follows: (1) claim 1 as unpatentable under 35 U.S.C. § 103(a) over Alsup in view of Meyer; and (2) claim 2 as anticipated under 35 U.S.C. § 102(b) by Alsup.


To better define the present invention, claims 1 and 2 have been cancelled and replaced with new claims 3 and 4. Both new claims 3 and 4 are cast as improvement in a microprocessor comprising a method for performing register renaming. The scope of claims 1 and 2 have been retained as new claims 3 and 4.

It is now clear that a large number of instructions per clock cycle are processed by register renaming in a pipelined manner unlike what is taught in either Alsup or Meyer. Notice in particular col. 9, lines 32 and 54 of Meyer's disclosures that Rename-2 unit receives only up to three instructions per clocks cycle.

Reconsideration of this application in view of the documentation of new claims 3 and 4 is respectfully requested.

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Respectfully submitted,  
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